This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “PIO 8255 (Programmable Input – Output Port)”.

1. Programmable peripheral input-output port is other name for
   a) serial input-output port
   b) parallel input-output port
   c) serial input port
   d) parallel output port

   Answer: b
   Explanation: The parallel input-output port chip 8255 is also known as programmable peripheral input-output port.

2. Port C of 8255 can function independently as
   a) input port
   b) output port
   c) either input or output ports
   d) both input and output ports

   Answer: c
   Explanation: Port C can function independently either as input or as output ports.

3. All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
   a) data bus control
   b) read logic control
   c) control word register
   d) none

   Answer: c
   Explanation: By programming the bits of control word register, the operations of the ports are specified.

4. The data bus buffer is controlled by
   a) control word register
   b) read/write control logic
   c) data bus
   d) none

   Answer: b
   Explanation: The data bus buffer is controlled by read/write control logic.
5. The input provided by the microprocessor to the read/write control logic is
   a) RESET
   b) A1
   c) WR(ACTIVE LOW)
   d) all of the mentioned

   Answer: d
   Explanation: RD(ACTIVE LOW), WR(ACTIVE LOW), A1, A0, RESET are the inputs provided by the microprocessor to the read/write control logic of 8255.

6. The device that receives or transmits data upon the execution of input or output instructions by the microprocessor is
   a) control word register
   b) read/write control logic
   c) 3-state bidirectional buffer
   d) none

   Answer: c
   Explanation: 3-state bidirectional buffer is used to receives or transmits data upon the execution of input or output instructions by the microprocessor.

7. The port that is used for the generation of handshake lines in mode 1 or mode 2 is
   a) port A
   b) port B
   c) port C Lower
   d) port C Upper

   Answer: d
   Explanation: Port C upper is used for the generation of handshake lines in mode 1 or mode 2.

8. If A1=0, A0=1 then the input read cycle is performed from
   a) port A to data bus
   b) port B to data bus
   c) port C to data bus
   d) CWR to data bus

   Answer: b
   Explanation: If A1=0, A0=1 then the input read cycle is performed from port B to data bus.

9. The function, ‘data bus tristated’ is performed when
   a) CS(active low) =1
   b) CS(active low) =0
c) CS(active low) = 0, RD(active low) = 1, WR(active low) = 1

d) CS(active low) = 1 OR CS(active low) = 0, RD(active low) = 1, WR(active low) = 1

Answer: d
Explanation: the data bus is tristated when chip select pin = 1 or chip select pin = 0 and read and write signals are high i.e 1.

10. The pin that clears the control word register of 8255 when enabled is
a) CLEAR
b) SET
c) RESET
d) CLK

Answer: c
Explanation: If reset pin is enabled then the control word register is cleared.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Interfacing I/O Ports”.

1. The device that enables the microprocessor to read data from the external devices is
a) printer
b) joystick
c) display
d) reader

Answer: b
Explanation: Since joystick is an input device, it reads data from the external devices.

2. The example of output device is
a) CRT display
b) 7-segment display
c) printer
d) all of the mentioned

Answer: d
Explanation: The output device transfers data from microprocessor to the external devices.

3. The input and output operations are respectively similar to the operations,
a) read, read
b) write, write
c) read, write
d) write, read

Answer: c
Explanation: The input activity is similar to read operation and the output activity is similar to write operation.

4. The operation, IOWR (active low) performs
a) write operation on input data
b) write operation on output data
c) read operation on input data
d) read operation on output data

Answer: b
Explanation: IOWR (active low) operation means writing data to an output device and not an input device.

5. The latch or IC 74LS373 acts as
a) good input port
b) bad input port
c) good output port
d) bad output port

Answer: c
Explanation: If the output port is to source large currents, the port lines must be buffered. So, the latch is used as it acts as good output port.

6. While performing read operation, one must take care that much current should not be
a) sourced from data lines
b) sunked from data lines
c) sourced or sunked from data lines
d) sunked from address lines

Answer: c
Explanation: More current should not be sourced or sunked from data lines while reading to avoid loading.

7. To avoid loading during read operation, the device used is
a) latch
b) flipflop
c) buffer
d) tristate buffer
Answer: d
Explanation: A tristate buffer is used as an input device to overcome loading.

8. The chip 74LS245 is
a) bidirectional buffer
b) 8-bit input port
c) one that has 8 buffers
d) all of the mentioned

Answer: d
Explanation: The chip 74LS245 is a bidirectional buffer that contains 8 buffers and may be used as an 8-bit input port. But while using as an input device, only one direction is useful.

9. In 74LS245, if DIR is 1, then the direction is from
a) inputs to outputs
b) outputs to inputs
c) source to sink
d) sink to source

Answer: a
Explanation: If DIR is 1, then the direction is from A(inputs) to B(outputs).

10. In memory-mapped scheme, the devices are viewed as
a) distinct I/O devices
b) memory locations
c) only input devices
d) only output devices

Answer: b
Explanation: In memory-mapped scheme, the devices are viewed as memory locations and are addressed likewise.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Modes of Operation of 8255”.

1. In the I/O mode, the 8255 ports work as
a) reset pins
b) set pins
c) programmable I/O ports
d) only output ports
Answer: c
Explanation: In the I/O mode, the 8255 ports work as programmable I/O ports.

2. In BSR mode, only port C can be used to
   a) set individual ports
   b) reset individual ports
   c) set and reset individual ports
   d) programmable I/O ports

Answer: c
Explanation: In BSR (Bit Set-Reset) Mode, port C can be used to set and reset its individual port bits.

3. The feature of mode 0 is
   a) any port can be used as input or output
   b) output ports are latched
   c) maximum of 4 ports are available
   d) all of the mentioned

Answer: d
Explanation: In mode 0, any port can be used as input or output and output ports are latched.

4. The strobed input/output mode is another name of
   a) mode 0
   b) mode 1
   c) mode 2
   d) none

Answer: b
Explanation: In this mode, the handshaking signals control the input or output action of the specified port.

5. If the value of the pin STB (Strobe Input) falls to low level, then
   a) input port is loaded into input latches
   b) input port is loaded into output latches
   c) output port is loaded into input latches
   d) output port is loaded into output latches

Answer: a
Explanation: If the value of the pin STB (Strobe Input) falls to low level, then input port is loaded into input latches.
6. The signal, SLCT in the direction of signal flow, OUT, indicates the selection of
   a) control word register
   b) CPU
   c) Printer
   d) ports

   Answer: c
   Explanation: This signal indicates that the printer is selected.

7. The pulse width of the signal INIT at the receiving terminal must be more than
   a) 10 microseconds
   b) 20 microseconds
   c) 40 microseconds
   d) 50 microseconds

   Answer: d
   Explanation: The pulse width of the signal must be more than 50 microseconds at the receiving terminal.

8. The level of the signal ERROR (active low) becomes ‘low’ when the printer is in
   a) Paper end state
   b) Offline state
   c) Error state
   d) all of the mentioned

   Answer: d
   Explanation: The level of the signal ERROR (active low) becomes ‘low’ when the printer is in Paper end state, Offline state and Error state.

9. The signals that are provided to maintain proper data flow and synchronisation between the
data transmitter and receiver are
   a) handshaking signals
   b) control signals
   c) input signals
   d) none

   Answer: a
   Explanation: Handshaking signals maintain proper data flow and synchronisation.

10. The feature of mode 2 of 8255 is
   a) single 8-bit port is available
   b) both inputs and outputs are latched
c) port C is used for generating handshake signals
d) all of the mentioned

Answer: d
Explanation: In mode 2 of 8255, single 8-bit port is available i.e group A.

ADC

1. The time taken by the ADC from the active edge of SOC(start of conversion) pulse till the active edge of EOC(end of conversion) signal is called
   a) edge time
   b) conversion time
   c) conversion delay
   d) time delay

Answer: c
Explanation: Broadly speaking, the time taken by the converter to calculate the equivalent digital data output from the moment of the start of conversion is called conversion delay.

2. The popular technique that is used in the integration of ADC chips is
   a) successive approximation
   b) dual slope integration
   c) successive approximation and dual slope integration
   d) none

Answer: c
Explanation: Successive approximation and dual slope integration are the most popular techniques that are used in the integrated ADC chips.

3. The procedure of algorithm for interfacing ADC contain
   a) ensuring stability of analog input
   b) issuing start of conversion pulse to ADC
   c) reading digital data output of ADC as equivalent digital output
   d) all of the mentioned

Answer: d
Explanation: The general algorithm for interfacing ADC contains ensuring stability of analog input, issuing start of conversion pulse to ADC, reading end of conversion signal to mark the end of conversion process, reading digital data output of ADC as equivalent digital output.
4. Which is the ADC among the following?
   a) AD 7523
   b) 74373
   c) 74245
   d) ICL7109

   Answer: d
   Explanation: AD 7523 is a DAC (Digital to analog converter), 74373 is a latch, 74245 is a transreceiver and ICL7109 is an ADC.

5. The conversion delay in successive approximation of an ADC 0808/0809 is
   a) 100 milliseconds
   b) 100 microseconds
   c) 50 milliseconds
   d) 50 milliseconds

   Answer: b
   Explanation: The conversion delay is 100 microseconds which is low as compared to other converters.

6. The number of inputs that can be connected at a time to an ADC that is integrated with successive approximation is
   a) 4
   b) 2
   c) 8
   d) 16

   Answer: c
   Explanation: As these converters internally have 3:8 analog multiplexer, at a time 8 different analog inputs can be connected to the chip.

7. ADC 7109 integrated by Dual slope integration technique is used for
   a) low cost option
   b) slow practical applications
   c) low complexity
   d) all of the mentioned

   Answer: d
   Explanation: Compared to other 12-bit ADCs, it is of very low cost and useful for slow practical applications.
8. Which of the following is not one of the phase of total conversion cycle?
   a) autozero phase
   b) conversion phase
   c) signal integrate phase
   d) deintegrate phase

   Answer: b
   Explanation: autozero phase, signal integrate phase and deintegrate phase are the three phases of total conversion cycle.

9. Which of the following phase contain feedback loop in it?
   a) autozero phase
   b) signal integrate phase
   c) deintegrate phase
   d) none

   Answer: a
   Explanation: A feedback loop is closed around the system to charge the autozero capacitor to compensate for the offset voltages in the buffer amplifier, integrator and comparator.

10. In the signal integrate phase, the differential input voltage between IN LO(input low) and IN HI(input high) pins is integrated by the internal integrator for a fixed period of
   a) 256 clock cycles
   b) 1024 clock cycles
   c) 2048 clock cycles
   d) 4096 clock cycles

   Answer: c
   Explanation: The internal integrator needs 2048 clock cycles to integrate voltage difference between input low and input high.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Interfacing Digital to Analog Converters, Stepper Motor Interfacing and Control of High Power Devices Using 8255”.

1. DAC (Digital to Analog Converter) finds application in
   a) digitally controlled gains
   b) motor speed controls
   c) programmable gain amplifiers
   d) all of the mentioned
Answer: d
Explanation: DAC is used in digitally controlled gains, motor speed controls and programmable gain amplifiers.

2. To save the DAC from negative transients the device connected between OUT1 and OUT2 of AD 7523 is
   a) p-n junction diode
   b) Zener
   c) FET
   d) BJT (Bipolar Junction transistor)

Answer: b
Explanation: Zener is connected between OUT1 and OUT2 pins of AD7523 to save from negative transients.

3. An operational amplifier connected to the output of AD 7523 is used
   a) to convert current output to output voltage
   b) to provide additional driving capability
   c) as current-to-voltage converter
   d) all of the mentioned

Answer: d
Explanation: An operational amplifier is used as a current-to-voltage converter to convert current output to output voltage and also provides additional driving capability to the DAC.

4. The DAC 0800 has a settling time of
   a) 100 milliseconds
   b) 100 microseconds
   c) 50 milliseconds
   d) 50 microseconds

Answer: a
Explanation: DAC 0800 has a settling time of 100 milliseconds.

5. The device that is used to obtain an accurate position control of rotating shafts in terms of steps is
   a) DC motor
   b) AC motor
   c) Stepper motor
   d) Servo motor
Answer: c
Explanation: Stepper motor employs rotation of its shaft in terms of steps, rather than continuous rotation as in case of AC or DC motors.

6. The internal schematic of a typical stepper motor has
   a) 1 winding
   b) 2 windings
   c) 3 windings
   d) 4 windings

   Answer: d
   Explanation: the internal schematic of a typical stepper motor has 4 windings.

7. The number of pulses required for one complete rotation of the shaft of the stepper motor is equal to the
   a) number of internal teeth on a rotor
   b) number of internal teeth on a stator
   c) number of internal teeth on a rotor and stator
   d) number of external teeth on a stator

   Answer: a
   Explanation: The number of pulses required for one complete rotation of the shaft of the stepper motor is equal to the number of internal teeth on its rotor.

8. A simple scheme for rotating the shaft of a stepper motor is called
   a) rotating scheme
   b) shaft scheme
   c) wave scheme
   d) none

   Answer: c
   Explanation: In this scheme, the windings are applied with the required voltage pulses, in a cyclic fashion.

9. The firing angles of thyristors are controlled by
   a) pulse generating circuits
   b) relaxation oscillators
   c) microprocessor
   d) all of the mentioned
Answer: d
Explanation: In early days, the firing angles were controlled by pulse generating circuits like relaxation oscillators and now, they are accurately fired using a microprocessor.

10. The Isolation transformers are generally used for
a) protecting low power circuit
b) isolation
c) protecting low power circuit and isolation
d) none

Answer: c
Explanation: Any switching component of a high power circuit may be sufficient to damage the microprocessor system. So, to protect the low power circuit isolation transformers are used. They are also used if isolation is necessary.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Programmable Interval Timer 8254”.

1. The number of counters that are present in the programmable timer device 8254 is
a) 1
b) 2
c) 3
d) 4

Answer: c
Explanation: There are three counters that can be used as either counters or delay generators.

2. The operation that can be performed on control word register is
a) read operation
b) write operation
c) read and write operations
d) none

Answer: b
Explanation: The control word register can only be written and cannot be read.

3. The mode that is used to interrupt the processor by setting a suitable terminal count is
a) mode 0
b) mode 1
c) mode 2
d) mode 3
Answer: a
Explanation: Mode 0 is also called as interrupt on terminal count.

4. In mode 2, if N is loaded as the count value, then after (N-1) cycles, the output becomes low for
a) 1 clockcycle
b) 2 clockcycles
c) 3 clockcycles
d) 4 clockcycles

Answer: a
Explanation: After (N-1) cycles, the output becomes low for only 1 clockcycle. If the count N is reloaded and again the output becomes high and remains so for (N-1) clock pulses.

5. The generation of square wave is possible in the mode
a) mode 1
b) mode 2
c) mode 3
d) mode 4

Answer: c
Explanation: When the count N loaded is even, then for half of the count, the output remains high and for the remaining half it remains low. If the count loaded is odd, the first clock pulse decrements it by 1 resulting in an even count value.

6. In control word register, if SC1=0 and SC0=1, then the counter selected is
a) counter 0
b) counter 1
c) counter 2
d) none

Answer: b
Explanation: SC denotes select counter.

7. In control word format, if RL1=1, RL0=1 then the operation performed is
a) read/load least significant byte only
b) read/load most significant byte only
c) read/load LSB first and then MSB
d) read/load MSB first and then LSB

Answer: c
Explanation: To access 16 bit, first LSB is loaded first, and then MSB.
8. If BCD=0, then the operation is
   a) decimal count
   b) hexadecimal count
   c) binary count
   d) octal count

   Answer: b
   Explanation: If BCD=0 then hexadecimal count. If BCD=1, then the operation is BCD count.

9. The counter starts counting only if
   a) GATE signal is low
   b) GATE signal is high
   c) CLK signal is low
   d) CLK signal is high

   Answer: b
   Explanation: If the GATE signal is enabled, then the counter starts counting.

10. The control word register contents are used for
    a) initialising the operating modes
    b) selection of counters
    c) choosing binary/BCD counters
    d) all of the mentioned

   Answer: d
   Explanation: The control word register contents are used for
   i) initialising the operating modes (mode 0-mode 4)
   ii) selection of counters (counter0-counter2)
   iii) choosing binary or BCD counters
   iv) loading of the counter registers.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “the Keyboard/Display Controller 8279”.

1. The registers that store the keyboard and display modes and operations programmed by CPU are
   a) I/O control and data buffers
   b) control and timing registers
   c) return buffers
   d) display address registers
Answer: b
Explanation: The control and timing registers store the keyboard and display modes and other operations programmed by CPU.

2. The sensor RAM acts as 8-byte first-in-first-out RAM in
a) keyboard mode
b) strobed input mode
c) keyboard and strobed input mode
d) scanned sensor matrix mode

Answer: c
Explanation: In this mode, each key code of the pressed key is entered in the order of the entry, and in the meantime, read by the CPU, till the RAM becomes empty.

3. The registers that holds the address of the word currently being written by the CPU from the display RAM are
a) control and timing register
b) control and timing register and timing control
c) display RAM
d) display address registers

Answer: d
Explanation: The display address registers holds the address of the word currently being written or read by the CPU to or from the display RAM.

4. When a key is pressed, a debounce logic comes into operation in
a) scanned keyboard special error mode
b) scanned keyboard with N-key rollover
c) scanned keyboard mode with 2 key lockout
d) sensor matrix mode

Answer: c
Explanation: In scanned keyboard mode with 2 key lockout mode of operation, when a key is pressed, a debounce logic comes into operation. During the next two scans, other keys are checked for closure and if no other key is pressed then the first pressed key is identified.

5. The mode that is programmed using “end interrupt/error mode set command” is
a) scanned keyboard special error mode
b) scanned keyboard with N-key rollover
c) scanned keyboard mode with 2 key lockout
d) sensor matrix mode
Answer: a  
Explanation: The scanned keyboard special error mode is programmed using end interrupt/error mode set command. This mode is valid only under the N-key rollover mode.

6. When a key is pressed, the debounce circuit waits for 2 keyboard scans and then checks whether the key is still depressed in  
a) scanned keyboard special error mode  
b) scanned keyboard with N-key rollover  
c) scanned keyboard mode with 2 key lockout  
d) sensor matrix mode

Answer: b  
Explanation: In this mode, When a key is pressed, the debounce circuit waits for 2 keyboard scans and then checks whether the key is still depressed. If it is still depressed, the code is entered in FIFO RAM.

7. The data that is entered from the left side of the display unit is of  
a) left entry mode  
b) right entry mode  
c) left and right entry modes  
d) none

Answer: a  
Explanation: The data that is entered from the left side of the display unit is of left entry mode, as in a type-writer the first character typed appears at the left-most position, while the subsequent characters appear successively to the right of the first one.

8. The FIFO status word is used to indicate the error in  
a) keyboard mode  
b) strobed input mode  
c) keyboard and strobed input mode  
d) scanned sensor matrix mode

Answer: c  
Explanation: Overrun error occurs, when an already full FIFO is attempted an entry. Underrun error occurs when an empty FIFO read is attempted.

9. The flag that increments automatically after each read or write operation to the display RAM is  
a) IF  
b) RF  
c) AI
d) WF

Answer: c
Explanation: AI refers to auto increment flag.

10. If any change in sensor value is detected at the end of a sensor matrix scan, then the IRQ line
a) goes low
b) goes high
c) remains unchanged
d) none

Answer: b
Explanation: In sensor matrix mode, the IRQ line goes high, if any change in sensor value is
detected at the end of a sensor matrix scan or the sensor RAM has a previous entry to be read by
the CPU.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on
“Programmable Communication Interface 8251 USART”.

1. Which of the following is not a mode of data transmission?
a) simplex
b) duplex
c) semi duplex
d) half duplex

Answer: c
Explanation: Basically, there are three modes of data transmission. simplex, duplex and half
duplex.

2. If the data is transmitted only in one direction over a single communication channel, then it is
of
a) simplex mode
b) duplex mode
c) semi duplex mode
d) half duplex mode

Answer: a
Explanation: In simplex mode, the data transmission is unidirectional. For example, a CPU may
transmit data for a CRT display unit in this mode.
3. If the data transmission takes place in either direction, but at a time data may be transmitted only in one direction then, it is of
   a) simplex mode
   b) duplex mode
   c) semi duplex mode
   d) half duplex mode

Answer: d
Explanation: In half duplex mode, data transmission is bidirectional but not at a time. For example, Walkie-Talkie.

4. In 8251A, the pin that controls the rate at which the character is to be transmitted is
   a) TXC(active low)
   b) TXC(active high)
   c) TXD(active low)
   d) RXC(active low)

Answer: a
Explanation: Transmitter Clock Input (TXC(active low)) is a pin that controls the rate at which the character is to be transmitted.

5. TXD(Transmitted Data Output) pin carries serial stream of the transmitted data bits along with
   a) start bit
   b) stop bit
   c) parity bit
   d) all of the mentioned

Answer: d
Explanation: Transmitted Data Output pin carries serial stream of the transmitted data bits along with other information like start bits, stop bits and parity bits etc.

6. The signal that may be used either to interrupt the CPU or polled by the CPU is
   a) TXRDY(Transmitter ready)
   b) RXRDY(Receiver ready output)
   c) DSR(active low)
   d) DTR(active low)

Answer: b
Explanation: RXRDY(Receiver ready output) may be used either to interrupt the CPU or polled by the CPU.
7. The disadvantage of RS-232C is
a) limited speed of communication
b) high-voltage level signaling
c) big-size communication adapters
d) all of the mentioned

Answer: d
Explanation: RS232C has been used for long and has a few disadvantages like limited speed of communication, high-voltage level signaling and big-size communication adapters.

8. The USB supports the signaling rate of
a) full-speed USB 1.0 at rate of 12 Mbps
b) high-speed USB 2.0 at rate of 480 Mbps
c) super-speed USB 3.0 at rate of 596 Mbps
d) all of the mentioned

Answer: d
Explanation: The USB standards support the signaling rates. Also, USB signaling is implemented in differential in low- and full-speed options.

9. The bit packet that commands the device either to receive data or transmit data in transmission of USB asynchronous communication is
a) handshake packet
b) token packet
c) PRE packet
d) data packet

Answer: b
Explanation: The token packet is a second type of packet which commands the device either to receive data or transmit data.

10. High speed USB devices neglect
a) handshake packet
b) token packet
c) PRE packet
d) data packet

Answer: c
Explanation: PRE packets are only of importance to low-speed USB devices.
This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “DMA Transfers and Operations”.

1. The 8237 is able to accomplish the operation of
   a) verifying DMA operation
   b) write operation
   c) read operation
   d) all of the mentioned

Answer: d
Explanation: The 8237 can accomplish three types of operations and they are
   i) verify DMA operation
   ii) write operation
   iii) read operation

2. The bus is available when the DMA controller receives the signal
   a) HRQ
   b) HLDA
   c) DACK
   d) all of the mentioned

Answer: b
Explanation: If the HLDA signal is received by the DMA controller, it indicates that the bus is available.

3. To indicate the I/O device that its request for the DMA transfer has been honoured by the CPU, the DMA controller pulls
   a) HLDA signal
   b) HRQ signal
   c) DACK (active low)
   d) DACK (active high)

Answer: c
Explanation: The DACK (active low) line of the used channel is pulled down by the DMA controller to indicate the I/O device that its request for the DMA transfer has been honoured by the CPU.

4. If more than one channel requests service simultaneously, the transfer will occur as
   a) multi transfer
   b) simultaneous transfer
   c) burst transfer
   d) none of the mentioned
Answer: c
Explanation: If more than one channel requests service simultaneously, then the transfer occurs as a burst or continuous transfer.

5. The continuous transfer may be interrupted by an external device by pulling down the signal
a) HRQ
b) DACK (active low)
c) DACK (active high)
d) HLDA

Answer: d
Explanation: The burst or continuous transfer may be interrupted by an external device by pulling down the HLDA line.

6. The number of clock cycles required for a 8237 to complete a transfer is
a) 2
b) 4
c) 8
d) none of the mentioned

Answer: b
Explanation: The 8237 uses four clock cycles to complete a transfer.

7. In 8237, if each device connected to a channel is assigned to a fixed priority then it is said to be in
a) rotating priority scheme
b) fixed priority scheme
c) rotating priority and fixed priority scheme
d) none of the mentioned

Answer: b
Explanation: In this scheme, the DRQ3 has the lowest priority followed by DRQ2 and DRQ1. The DRQ0 has the highest priority.

8. The priority of the channels varies frequently in
a) rotating priority scheme
b) fixed priority scheme
c) rotating priority and fixed priority scheme
d) none of the mentioned

Answer: a
Explanation: In this scheme, the priorities assigned to the channels are not fixed.
9. The register of 8237 that can only be written in is
a) DMA address register  
b) terminal count register  
c) mode set register  
d) status register

Answer: c  
Explanation: The selected register may be read or written depending on the instruction executed by the CPU. But only write operation can be performed on the mode set register.

10. The operation that can be performed on the status register is
a) write operation  
b) read operation  
c) read and write operations  
d) none of the mentioned

Answer: b  
Explanation: The status register can only be read.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Programmable DMA Interface 8237 -1”

1. The block of 8237 that decodes the various commands given to the 8237 by the CPU is
a) timing and control block  
b) program command control block  
c) priority block  
d) none of the mentioned

Answer: b  
Explanation: The program control block decodes various commands given to the 8237 by the CPU before servicing a DMA request.

2. The priority between the DMA channels requesting the services can be resolved by
a) timing and control block  
b) program command control block  
c) priority block  
d) none of the mentioned

Answer: c  
Explanation: The priority encoder block resolves the priority between the DMA channels requesting the services.
3. The register that holds the current memory address is
   a) current word register
   b) current address register
   c) base address register
   d) command register

   Answer: b
   Explanation: The current address register holds the current memory address. The current address register is accessed during the DMA transfer.

4. The register that holds the data byte transfers to be carried out is
   a) current word register
   b) current address register
   c) base address register
   d) command register

   Answer: a
   Explanation: The current word register is a 16-bit register that holds the data transfers. The word count is decremented after each transfer, and the new value is stored again in the register.

5. When the count becomes zero in the current word register then
   a) input signal is enabled
   b) output signal is enabled
   c) EOP (end of process) is generated
   d) start of process is generated

   Answer: c
   Explanation: When the count becomes zero, the EOP signal is generated. This can be written in successive bytes by the CPU, in program mode.

6. The current address register is programmed by the CPU as
   a) bit-wise
   b) byte-wise
   c) bit-wise and byte-wise
   d) none of the mentioned

   Answer: b
   Explanation: The current address register is byte-wise programmed by the CPU, i.e. lower byte first and the higher byte later.

7. Which of these register’s contents is used for auto-initialization (internally)?
   a) current word register
b) current address register  
c) base address register  
d) command register

Answer: c  
Explanation: The contents of base address register cannot be read by the CPU. These contents are used internally for auto-initialization.

8. The register that maintain an original copy of the respective initial current address register and current word register is  
a) mode register  
b) base address register  
c) command register  
d) mask register

Answer: b  
Explanation: The base address register maintains an original copy of current address register and current word register, before incrementing or decrementing.

9. The register that can be automatically incremented or decremented, after each DMA transfer is  
a) mask register  
b) mode register  
c) command register  
d) current address register

Answer: d  
Explanation: The address is automatically incremented or decremented after each DMA transfer, and the resulting address value is again stored in the current address register.

10. Which of the following is a type of DMA transfer?  
a) memory read  
b) memory write  
c) verify transfer  
d) all of the mentioned

Answer: d  
Explanation: Memory read, memory write and verify transfer are the three types of DMA transfer.

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Programmable DMA Interface 8237 -2”
1. Each bit in the request register is cleared by
   a) under program control
   b) generation of TC
   c) generation of an external EOP
   d) all of the mentioned

   Answer: d
   Explanation: In the request register, each bit is set or reset under program control or is cleared upon generation of a TC or an external EOP.

2. The register that holds the data during memory to memory data transfer is
   a) mode register
   b) temporary register
   c) command register
   d) mask register

   Answer: b
   Explanation: The temporary register holds the data during memory to memory data transfers. After the completion of the transfer operation, the last word transferred remains in the temporary register, till it is cleared by a reset operation.

3. The register that keeps track of all the DMA channel pending requests, and status of their terminal counts is
   a) mask register
   b) request register
   c) status register
   d) count register

   Answer: c
   Explanation: The status register keeps track of all the DMA channel pending requests, and status of their terminal counts. These are cleared upon reset.

4. The pin that clears the command, request and temporary registers, and internal first/last flipflop when it is set is
   a) CLEAR
   b) SET
   c) HLDA
   d) RESET

   Answer: d
   Explanation: A high on the reset pin clears the command, status, request and temporary registers, and also clears the internal first/last flipflop.
5. The DMA request input pin that has the highest priority is
   a) DREQ0
   b) DREQ1
   c) DREQ2
   d) DREQ3

   Answer: a
   Explanation: DREQ0 has the highest priority while DREQ3 has the lowest one. The priorities of
   the DREQ lines is programmable.

6. When interface 8237 does not have any valid pending DMA request then it is said to be in
   a) active state
   b) passive state
   c) idle state
   d) none of the mentioned

   Answer: c
   Explanation: If 8237 is in idle state, then CPU may program it in this state.

7. To complete a DMA transfer, a memory to memory transfer requires
   a) a read from memory cycle
   b) a write to memory cycle
   c) a read-from and write-to memory cycle
   d) none of the mentioned

   Answer: c
   Explanation: A memory to memory transfer is a two cycle operation, and requires a read from
   and write-to memory cycle, to complete each DMA transfer.

8. In demand transfer mode of 8237, the device stops data transfer when
   a) a TC (terminal count) is reached
   b) an external EOP (active low) is detected
   c) the DREQ signal goes inactive
   d) all of the mentioned

   Answer: d
   Explanation: In demand transfer mode, the device continues transfers till a TC is reached or an
   external EOP is detected or the DREQ signal goes inactive.

9. The mode of 8237 in which the device transfers only one byte per request is
   a) block transfer mode
   b) single transfer mode
c) demand transfer mode
d) cascade mode

Answer: b
Explanation: In single mode, the device transfers only one byte per request. For each transfer, the DREQ must be active until the DACK is activated.

10. The transfer of a block of data from one set of memory address to another takes place in
a) block transfer mode
b) demand transfer mode
c) memory to memory transfer mode
d) cascade mode

Answer: c
Explanation: To perform the transfer of a block of data from one set of memory address to another one, this transfer mode is used.

11. Which of the following command is used to make all the internal registers of 8237 clear?
a) clear first/last flipflop
b) master clear command
c) clear mask register
d) none of the mentioned

Answer: b
Explanation: Using master clear command, all the internal registers of 8237 are cleared, while all the bits of the mask register are set.